

Amendments to the Claims:

The following Listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A laminated flip-chip interconnect package comprising a substrate having a chip attach surface and an opposing board attach surface that define contact pads for attachment to corresponding pads on the chip and board, wherein the board attach surface comprises a pattern of contact pads opposite and adjacent to a chip attach location on the chip attach surface except at least one unpatterned solid plane area of the board attach surface, said unpatterned solid plane area being adjacent to a corner of a chip attach location, and said board attach surface comprising a dielectric material, wherein the unpatterned solid plane area ~~is at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area~~ extends a distance equal to at least two contact pad rows beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to one contact pad row.
2. (Previously presented) A laminated flip-chip interconnect package according to claim 1 wherein said dielectric material is covered with a layer of material selected from a solder mask and a coverlay material.
3. (Original) A laminated flip-chip interconnect package according to claim 2 wherein said layer of material is selected from the group consisting of polyimide, polytetrafluoroethylene, and expanded polytetrafluoroethylene impregnated with cyanate ester and epoxy.
4. (Currently Amended) A laminated flip-chip interconnect package comprising a substrate having a chip attach surface and an opposing board attach surface that defines a pattern of contact pads for attachment to corresponding pads on the chip and board, wherein the board attach surface comprises at least one unpatterned solid plane area, said unpatterned

area being opposite a chip attach surface region adjacent at least one corner of a chip attach location, and said board attach surface comprising a metal, wherein the unpatterned solid plane area is ~~at least the size of a region in which strain due to thermal cycling from 125°C to -55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area~~ extends a distance equal to at least two contact pad rows beyond the corner of the chip attach location for a distance equal to at least two contact pad rows and extends under the corner of the chip attach location for a distance equal to one contact pad row.

5. (Original) A laminated flip-chip interconnect package according to claim 4 wherein said metal is selected from the group consisting of copper, silver, gold and aluminum.
6. (Previously presented) A laminated flip-chip interconnect package according to claim 4 wherein said metal is covered with a layer of material selected from a solder mask and a coverlay material.
7. (Original) A laminated flip-chip interconnect package according to claim 6 wherein said layer of material is selected from the group consisting of polyimide, polytetrafluoroethylene, and expanded polytetrafluoroethylene impregnated with cyanate ester and epoxy.
8. (Previously presented) A laminate flip-chip interconnect package according to claim 4 wherein a solder mask has a plurality of openings defining ball grid array pads.